Notice of Allowability	Application No.	Applicant(s)	
	09/888,189	KRISHNAN, SIVARAM	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *July 19, 2006*.

2. ☒ The allowed claim(s) is/are *1,3,5,6,10,12,14,15,17 and 18*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' communication dated July 19, 2006. Claims 1, 5, 10, 14, 15, 17 and 18 were amended. Claims 2 and 11 were canceled. Claims 1, 3, 5, 6, 10, 12, 14, 15, 17 and 18 of the application are pending.

Reasons for Allowance

2. Claims 1, 3, 5, 6, 10, 12, 14, 15, 17 and 18 of the application are allowed over prior art of record.

3. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) systems and methods for automated design verification of circuit designs using a test bench and test vectors; software models of the circuit design are used for design verification; the design verification uses a functional model for functional simulation; the model receives test vectors from the test generator, output data from the simulated design and verify output data's accuracy; the output data are compared against a set of expected values generated by the functional model; the output data are then labeled as correct or incorrect; the functional model is

a non-cycle accurate model of the simulated design; another software model used for design verification is the cycle accurate model; the cycle accurate model is coupled to receive test vectors from the test generator and to match cycle-for-cycle the output data from the simulated design; an output sequence comparator receives the output data from the simulated design and the cycle accurate model; the output sequence comparator compares every cycle the output data and labels the output data as correct or incorrect (**McNamara et al.,** U.S. Patent 6,687,662);

(2) a system level functional simulation technique for design verification of an LSI; high speed is required in simulation for functional verification; two alternative simulation methods used are event-driven simulation and cycle-based simulation; in event driven simulation, the signal value changes are monitored and changes in circuit status are calculated; in cycle based simulation, using a clock signal as a reference, all changes in the status of the circuit are calculated in relation to the signal value transition of the clock signal each clock cycle; the method performs simulation with a small scale test vector for a test before simulation with a desired test vector; simulation method to be used for the full simulation with the desired test vector is determined based on the event incident frequency of each functional module of the LSI (**Mizuno et al.,** U.S. Patent 6,370,494); and

(3) a co-simulation system that runs on a host computer includes a hardware simulator and a target processor simulator coupled via an interface mechanism; the execution of a user program is simulated by executing an analyzed version of the user program; the analysis adds timing information to the user program; the processor model can include more or less detail; the processor simulator accumulates simulation time delay determined using timing information that accounts for instruction timing including pipeline effects; when greater accuracy is desired than

provided by running the program on the host computer system, those aspects of the target processor's execution requiring greater accuracy may be modeled in hardware; the hardware is then simulated by the hardware simulator; the user may select the level of modeling accuracy; when greater speed is required the processor may be used to simulate the function or to provide pre-calculated values of delays involved in bus access and memory access (**Hellestrand et al.,** U.S. Patent 6,230,114).

None of these references taken either alone or in combination with the prior art of record discloses a method of simulating a system, specifically including:

(Claim 1) "in a simulator, performing simulation in a functional simulation mode having a first accuracy level for at least a first portion of code comprising the first portion of the system model, the behavior of the system represented by the first portion of code being simulated in the functional simulation mode without regard to execution time to thereby obtain information about functionality of the first portion of the simulated system; and

in the same simulator, performing simulation in a performance simulation mode having a second accuracy level different from the first accuracy level for at least a second portion of code comprising the second portion of the system model, the behavior of system represented by the second portion of code being simulated in the performance simulation mode, with regard to execution time to thereby obtain information about the performance of the second portion of the simulated system".

None of these references taken either alone or in combination with the prior art of record discloses a simulation system for simulating the performance of an external system, specifically including:

(Claim 10) "a module for performing simulation in a functional simulation mode having a first accuracy level for at least a first portion of code that models at least a first portion of the external system, the behavior of the first portion of the external system modeled by the first portion of code being simulated in the functional simulation mode without regard to execution time to thereby obtain information about functionality of the first portion of the external system; and

a module for performing simulation in a performance simulation mode having a second accuracy level different from the first accuracy level for at least a second portion of code that models at least a second portion of the external system, the behavior of the second portion of the external system modeled by the second portion of code being simulated in the performance simulation mode with regard to execution time to thereby obtain information about the performance of the second portion of the external system".

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

K. Thangavelu
Art Unit 2123
August 8, 2006